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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,165	01/18/2002	Katsuhiko Fukasaku	NE253-US	7604

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,165	FUKASAKU, KATSUHIKO	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7,8 and 11-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,8 and 11-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ono (US 6432776).

Regarding claim 22, Fig. 11 of Ono shows a semiconductor device comprising:

a plurality of transistors having different gate insulator film thickness values [131, 132], said plurality of types of transistors having different thickness values of a gate electrode [141, 142] thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said plurality of transistors comprise a plurality of sidewalls [19], a first lightly doped drain region [51], and a second lightly doped drain region [52], where said first lightly doped drain region and said second lightly doped drain region are formed using said plurality of sidewalls and said gate electrode as a mask [col. 4, line 51- col. 5, line 18], and

wherein said first and second lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.

Also, note that "formed using said plurality of sidewalls and said gate electrode as a mask" is a process designation and would thus not carry patentable weight in his claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 24, Fig. 11 of Ono shows a semiconductor device comprising:

a plurality of transistors comprising different gate insulator films [131, 132] in their thickness value, said plurality of transistors having different thickness values of gate electrode [141, 142] in correspondence to the thickness values of the gate insulator film thereof,

wherein said plurality of transistors comprise a plurality of MOSFETs [col. 1, lins2-5] formed on a substrate [11],

wherein said plurality of MOSFETs comprise a core-purpose MOSFET and an 1/0purpose MOSFET, and

wherein said core-purpose MOSFET has a smaller thickness of the gate insulator film than that of said 1/0-purpose MOSFET and has a smaller thickness of the gate electrode than that of said 1/0-purpose MOSFET, and also has smaller depths of lightly doped drain regions of said core-purpose MOSFET than that of said 1/0-purpose MOSFET.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7, 8 11-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Chien et al. (US 6432768), hereinafter Chien.

Regarding claim 1, Fig. 11 of Ono shows a semiconductor device comprising:

a plurality of transistors comprising different gate insulator film [131, 132] in their thickness value, said plurality of transistors having different thickness values of a gate electrode [141, 142] thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said plurality of transistors comprise lightly doped drain regions, [51, 52], and

wherein said lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.

Fig. 11 of Ono shows substantially the entire claimed structure except "said gate electrode includes an impurity to suppress depletion." Fig. 1C of Chien shows a semiconductor device with a gate electrode [124] including an impurity (doped polysilicon; col. 2, line 45).

It would have been obvious to one of ordinary skill to use the teachings of Chien to the device of Ono in order to have said gate electrode including an impurity, resulting in suppression of depletion to improve the device performance.

Regarding claim 2, Fig. 11 of Ono shows said plurality of transistors comprise a plurality of MOSFETs [col. 1, lines 2-5] formed on a substrate [11].

Regarding claims 3 and 11-12, Fig. 11 of Ono shows said plurality of MOSFETs includes a core-purpose MOSFET and an 1/O purpose MOSFET, and wherein said

core-purpose MOSFET has a smaller thickness of said gate insulator film than that of said 1/O-purpose MOSFET and also has a smaller thickness of said gate electrode than that of said 1/0-purpose MOSFET.

Regarding claim 7, Fig. 11 of Ono shows said plurality of transistors comprise another lightly doped drain region [51, 52].

Regarding claim 8, Fig. 11 of Ono shows said lightly doped drain region is deeper than said another lightly doped drain region.

Regarding claim 13, Ono discloses that core-purpose MOSFET comprises an N - channel MOSFET [col. 5, lines 50-54], but fails to disclose that wherein said core-purpose MOSFET comprises an N - channel MOSFET for being driven on a supply voltage of about 1.0v. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the core N-MOSFET being driven on a supply voltage of about 1.0v for fast operation , since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 14, Ono discloses that said 1/O-purpose MOSFET comprises an N - channel MOSFET [col. 5, lines 50-54], for being driven on a supply voltage of about 3,3v [col. 3, lines 65-68].

Regarding claim 15, Fig. 11 of Ono shows one of said lightly doped drain regions comprises an 1/O-purpose P-well [13] with an N - type impurity at a predetermined density and a predetermined energy level, wherein said N - type impurity comprises phosphorous [col. 4, lines 54-56].

Regarding claim 16, Ono fails to disclose that wherein said predetermined density is about 2 x $10^{13}/cm^2$, and wherein said predetermined energy level is about 30 keV. However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have said predetermined density about 2 x $10^{13}/cm^2$ with the predetermined energy level is about 30 keV to achieve a design-specific doping concentration, since it has been that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 17 and 20, Fig. 11 of Ono shows one of said another lightly doped drain regions comprises a core-purpose P-well [13] with an N - type impurity implanted at a predetermined density and a predetermined energy level, wherein said N - type impurity comprises arsenic [col. 4, lines 62-68].

Regarding claim 18, Ono fails to disclose that wherein said predetermined density is about 5 x $10^{14}/cm^2$, and wherein said predetermined energy level is about 2.5 keV. However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have said predetermined density about 5 x $10^{14}/cm^2$ with the predetermined energy level is about 2.5 keV to achieve a design-specific doping concentration, since it has been that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 19, Fig. 11 of Ono shows said plurality of transistors comprise a plurality of sidewalls, said plurality of sidewalls comprising a first sidewall and a second

sidewall, and wherein said first sidewall has a height greater than that of said second sidewall.

Regarding claim 21, Ono fails to disclose that wherein said predetermined density is about 5 x $10^{15}/cm^2$, and wherein said predetermined energy level is about 30 keV. However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have said predetermined density about 5 x $10^{15}/cm^2$ with the predetermined energy level is about 30 keV to achieve a design-specific doping concentration, since it has been that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 23, Fig. 11 of Ono shows a semiconductor device comprising:

a plurality of transistors having different gate insulator film thickness values [131, 132] said plurality of transistors having different thickness values of a gate electrode [141, 142] thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said thickness of said gate insulator film varies based on the amount of deposited gate electrode materials,

wherein said plurality of transistors comprise a plurality of sidewalls [19], and lightly doped drain regions [51, 52] formed using said plurality of sidewalls and said gate electrode as a mask [col. 4, line 51- col. 5, line 18], and

wherein said lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.

Fig. 11 of Ono shows substantially the entire claimed structure except the gate electrodes with a polysilicon film layer. Fig. 1C of Chien shows a semiconductor device with the gate electrodes [112,124] formed with polysilicon.

It would have been obvious to one of ordinary skill to use the teachings of Chien to the device of Ono in order to have the polysilicon gate electrodes to reduce the process steps.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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